Three-Phase Multi-pulse Converter Based on FPGA

Ausencio Cardona L., Omar Aguilar M., Ruben Tapia O., Felipe Coyotl M.

***Abstract*—The voltage source converter topology has gained wide acceptance for applications in electric power generation, motor drives, computer's power adapters, uninterruptible power supplies, flexible ac transmission systems, and alternative energy production systems. Therefore, it is necessary to understand clearly how they work and explore control techniques to improve its performance characteristics. This paper is aimed to present the analysis of steady state converter operation in laboratory prototype. The device is based on full bridge with twelve insulated gate bipolar transistor, including independent trigger signal for each element. The sinusoidal pulse width modulation technique is employed for regulating purpose programmed on FPGA. Finally, a comparison between digital simulations and experimental results is presented. The resultant alternating current waveform has a very well quality shape.**

***Index Terms*—Full bridge, harmonics, pulse width modulation, voltage source converter.**

I. Introduction

NOWADAYS in several applications for power electronic circuits are used, like electric power converters which transform the voltage from one type to another (DC-AC or AC-DC). These devices are known as Voltage Source Converters (VSC), where Pulse Width Modulation (PWM) control technique is widely used. Interfacing circuits deal with power and control stages, using power semiconductor that operate at high frequencies. They become in different topologies and functions for a variety of applications such as motor drives, computer's power adapters, Uninterruptible Power Supplies (UPS), Flexible AC Transmission Systems (FACTS), and alternative energy production systems [1-3]. Generate an AC voltage from a DC one is the major VSC aim, for that it is often referred to as a DC–AC converter or inverter. It is able to obtain a symmetric or asymmetric AC power with a desired magnitude and frequency that can be fixed or varied according to the request.

Currently, there are a large number of VSC's configurations divided mainly in two groups: a) multi-pulse and b) multilevel. To minimize voltage converter harmonics in the literature different kinds of topologies have been proposed. A detailed mathematical analysis for 6, 12, 24 and 48 pulses VSC's structure is done in [2], which shows that increasing the pulses number the harmonic content of the output voltage is reduced. However, VSC's that used a multi-pulse configuration make the harmonics cancellation in the secondary windings of coupling transformer, it becomes the main disadvantage.

In recent years, multilevel inverter has received considerable attention and has been widely recommended for high and medium power applications. This is due to its ability for generating voltage signals with minimum harmonic content, feature that favors the operation in special cases such as interconnection to the electric grid [3-5]. The main drawback that affects the multilevel VSC performance is the unbalance voltage between the capacitors of each level. Moreover, the failure probabilities of one or more switching devices in the implementation procedure are significantly increased when comparing with a multi-pulse configuration [6-8].

With the advancement on solid-state technology and intelligent devices it has been possible to overcome these disadvantages. For instance, the intelligent devices and software integration into electric systems control have been possible improved diagnostics, early warnings for increasing system reliability, design flexibility, and simplified wiring [9-11]. Effective uses of these strategies can reduce maintenance costs, minimize downtime, and offer opportunities for improving the electrical utilities safety.

Otherwise, the Sinusoidal Pulse Width Modulation (SPWM) technique is used due to its easy switching frequency adjustment, as well as, the distortion factor and harmonic content is low order, and therefore, can significantly reduce with a filter adjusted properly [12]. For example, the conventional structure of the three-phase VSC, Fig. 1, can be controlled independently as a single-phase inverter in order to have better control at each phase. It has six switching elements and eight discrete states of output voltage, where the pulses number in each trigger signal cycle depends on the carrier signal of each leg.

Comparing the performance of the triangular intersection technique [13] and the direct digital pulse programming technique [14], against carrier-based PWM methods the last one provides a linear relationship between the reference and output voltage. The voltage control level of VSC by SPWM is based mainly through the modulator characteristics.

This paper proposed to improve the VSC performance with a detailed implementation of SPWM control technique based on FPGA. It allows a three-phase sinusoidal waveform with independent phase regulator, and high signal quality for different cases maintaining a low harmonic index.

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II. Control Scheme

The pulse width modulation has been widely employed as a strategy for the voltage source converter operation, through the appropriate power electronic switches management, Fig. 1.

The PWM strategy provides the controlled commutation signals by variable pulses width. Typically, these are low power signals from a controller. In this paper a digital SPWM algorithm is implemented based on FPGA device, so that the pulses amplitude is maintained constant with different duty cycle for each period, Fig. 2. The pulses width is modulated to obtain inverter output voltage controlled, and reduce its harmonic content. To achieve a good behavior it possesses a 3-kHz frequency for carrier signal.

The pulse width modulation is accomplished by means of a comparator which generates the signals that command the switches. The comparator sends to the switch turn-on when the modulated signal (sine wave) is greater than the carrier one; otherwise, remains opened. In this paper, the carrier signal is triangular, and the PWM frequency depends on a modulated signal that acts as a reference, Fig. 2a.

The most common PWM technique for voltage source converters is sinusoidal pulse-width modulation. In the following the PWM principle will be explained. Three-phase reference sinusoidal voltages v_a, v_b, and v_c with amplitude, A, are compared in six independent stages with a triangular (isosceles) carrier wave, v_T, of an amplitude, A_c. For illustrative purpose the single-phase PWM is presented in Fig. 2a.

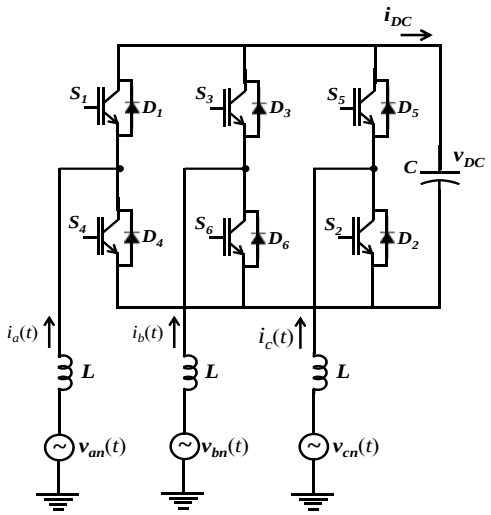
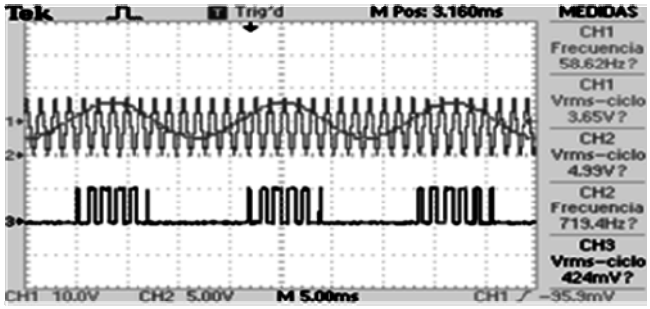
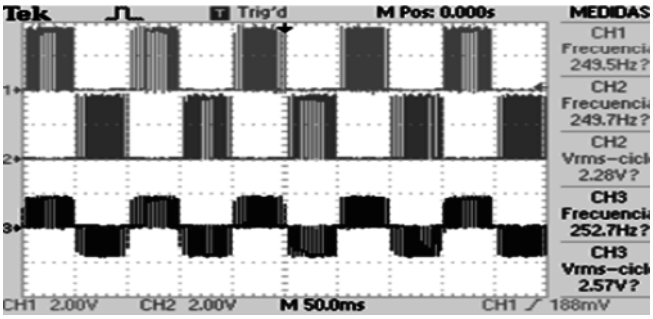


Fig. 1. Six pulse voltage source converter with star-connection.

The modulation is called sinusoidal PWM because the pulse width is a sinusoidal function of its angular position in the cycle. It is also known as triangulation or PWM with natural sampling. To generate a sinusoidal signal, the switches must be controlled in a certain sequence to create an output voltage waveform in a VSC. Therefore, a reference with similarity waveform is required as exhibits in Fig. 2a. However, the reference signal may come in various shapes to suit the converter topology, such as sine wave or distorted. A sinusoidal signal is used for PWM in DC to AC converter to establishment the output voltage shape and frequency. These signals are employed to trigger the four Insulated Gate Bipolar Transistor (IGBT) of the full single-phase bridge structure, Fig. 3.



(a)



(b)

Fig. 2. Transforming the desired continuous signal into SPWM: (a) SPWM process; (b) switching function.

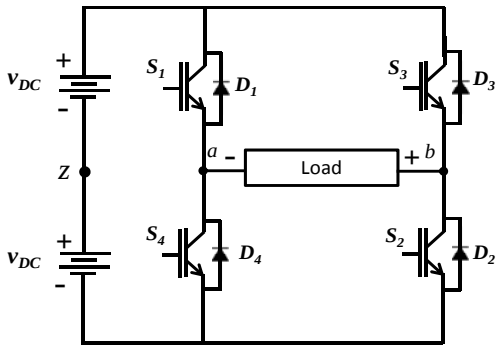


Fig. 3. Full single-phase bridge inverter topology.

A full single phase bridge inverter circuit and its output load are shown in Fig. 3. It consists of four switching elements and is used in higher power ratings application. The firing commands are labeled as S_1, S_2, S_3 and S_4. The full single phase bridge converter operation can be divided into two conditions: 1) normally the switches S_1 and S_4 are turned on and kept on for one half period, S_2 and S_3 are turned off, at this condition, the output voltage across the load is equal to v_{DC}; 2) when S_2 and S_3 are turned on, the switches S_1 and S_4 are turned off, then, the output voltage is equal to $-v_{DC}$. The terminal voltage will change alternately from positive to negative half period. Within the constraint that two transistors of the same leg (S_1 and S_4) cannot conduct at the same time. In order to prevent short circuit occurred, dead time mechanism has been carefully programmed in gate driver circuit. It is achieved if the SPWM algorithm is real time programming.

III. Converter Configuration

A. *Single-phase converter configuration*

Fig. 3 shows the full single-phase bridge structure of a VSC. Essentially, it is made up of two single legs connected to a common DC bus. Each is modulated in a

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complementary pattern by a carrier/reference waveform comparison circuit. The particular carrier and reference waveform depends on the PWM strategy implemented.

Both phase legs use a common carrier signal, Fig. 2a, and are modulated with 180° opposed reference waveforms, defined as

$$v_{az}^{*} = v_{DC}Mcos(\omega_0 t) \quad (1)$$

$$v_{bz}^{*} = v_{DC}Mcos(\omega_0 t - \pi) \quad (2)$$

where M is modulation index, and ω_0 is the target output angular frequency and v_{DC} is the DC input bus. Each phase leg reference wave considers to the DC bus voltage midpoint as a reference. The fundamental line to line converter output voltage is the difference between the two-phase leg reference voltages, and is given by

$$v_{ab}^{*} = v_{az}^{*} - v_{bz}^{*} = 2v_{DC}Mcos(\omega_0 t) \quad (3)$$

This arrangement achieves three-level naturally sampled SPWM, which has significant advantages over most other single-phase converter modulation strategies in appearance to eliminate undesirable low order harmonics (5th and 7th order) [12]. But it is by no means mandatory to use a common carrier for both phase legs, and even two sinusoidal reference waveforms.

Fig. 2b presents the three-level sampled PWM process for a single-phase inverter. It can be seen how each phase leg of the inverter switches between the upper and lower DC rails, continuously over the fundamental cycle as the carrier waveform ramps above and below the reference waveform. Note that the switched output voltage takes on values, $+v_{DC}$, and zero during the positive; and $-v_{DC}$ and zero during the negative period of the reference. This is due because the PWM arrangement is called three-level modulation, since the converter output voltage switches between three levels complete a fundamental cycle.

The harmonic solution for double-edge naturally sampled PWM has already been established in [15] by setting $\theta_0 = 0$ and $\theta_0 = -\pi$, for each phase legs a &b, respectively,

$$v_{az}^{*}(t) = v_{DC} + v_{DC}Mcos(\omega_0 t) + \frac{4v_{DC}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_n\left(m\frac{\pi}{2}M\right)sin\left([m+n]\frac{\pi}{2}\right) cos(m\omega_c t + n[\omega_0 t]) \quad (4)$$

$$v_{bz}^{*}(t) = v_{DC} + v_{DC}Mcos(\omega_0 t - \pi) + \frac{4v_{DC}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_n\left(m\frac{\pi}{2}M\right)sin\left([m+n]\frac{\pi}{2}\right) cos(m\omega_c t + n[\omega_0 t - \pi]) \quad (5)$$

ω_c is carrier angular frequency.

The arbitrary carrier phase angle in both cases has been set to zero for convenience, since it is the same for both phase legs. The output voltage harmonic components for the inverter are given by $v_{ab} = v_{an} - v_{bn}$, and can be developed from (4) and (5) [15],

$$v_{ab}(t) = 2v_{DC}Mcos(\omega_0 t) + \frac{8v_{DC}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{2m}J_{2n-1}(m\pi M) cos([m+n-1]\pi)cos(2m\omega_c t + [2n-1]\omega_0 t) \quad (6)$$

(6) shows that the odd carrier and associated sideband harmonic are completely cancelled from output voltage pulse train, leaving only odd sideband harmonic ($2n$-1) terms of the even ($2m$) carrier groups.

B. Three-phase converter configuration

The three-phase basic configuration is called six-pulse inverter, consisting of six asymmetric turn-off devices, such as GTO or IGBT, with reverse-parallel diodes connected as a six-pulse Graetz bridge, Fig. 1 [1]. The inverter can be seen as set up by three single-phase converters, where each phase produces an output voltage phase-shifted by ±120° with respect to the others.

In this work the three-phase converter topology is shown in Fig. 4. The essential difference compared to single-phase inverter is that two phase legs have been added, and, the reference sinusoidal for each phase leg is now displaced by 120°, not 180°. Using the same strategy that was used for single-phase inverter, we can find the solution to the converter output voltage per phase as [15],

$$v_{ab}(t) = \sqrt{3}v_{DC}Mcos\left(\omega_0 t + \frac{\pi}{6}\right) + \frac{8v_{DC}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_n\left(m\frac{\pi}{2}M\right)sin\left([m+n]\frac{\pi}{2}\right) sin\left(n\frac{\pi}{3}\right)cos\left(m\omega_c t + n\left[\omega_0 t - \frac{\pi}{3}\right] + \frac{\pi}{2}\right) \quad (7)$$

The higher pulse configuration purpose is to reduce the harmonic content of the resulting voltage waveforms. In the 12-pulse configuration the harmonic content is in the order of $n = 12m \pm 1$, where $m = 0, 1, 2, 3, \ldots$ [2].

A LC filter has been designed in order to limit the harmonic content in the output voltages. Coupling transformers are connected to the low pass filter, in a star-delta configuration, Fig. 4. As previously mentioned modulation is achieved using a sinusoidal control signal to the desired output frequency $f_0 = 60$ Hz. The gating signals Fig. 2a. are generated by comparing a sinusoidal reference signal with a triangular carrier wave of frequency f_c. The frequency of reference signal f_r determines the inverter output frequency f_o, and its peak amplitude A_r controls the modulation index M. The number of pulses per half-cycle is found from

$$P = \frac{f_c}{2f_0} = \frac{M}{2} \quad (8)$$

IV. Simulation Prototype

To know the performance of full single-phase bridge converter, several simulations were made in Proteus® software, evaluating the AC voltage waveform for different RLC loads.

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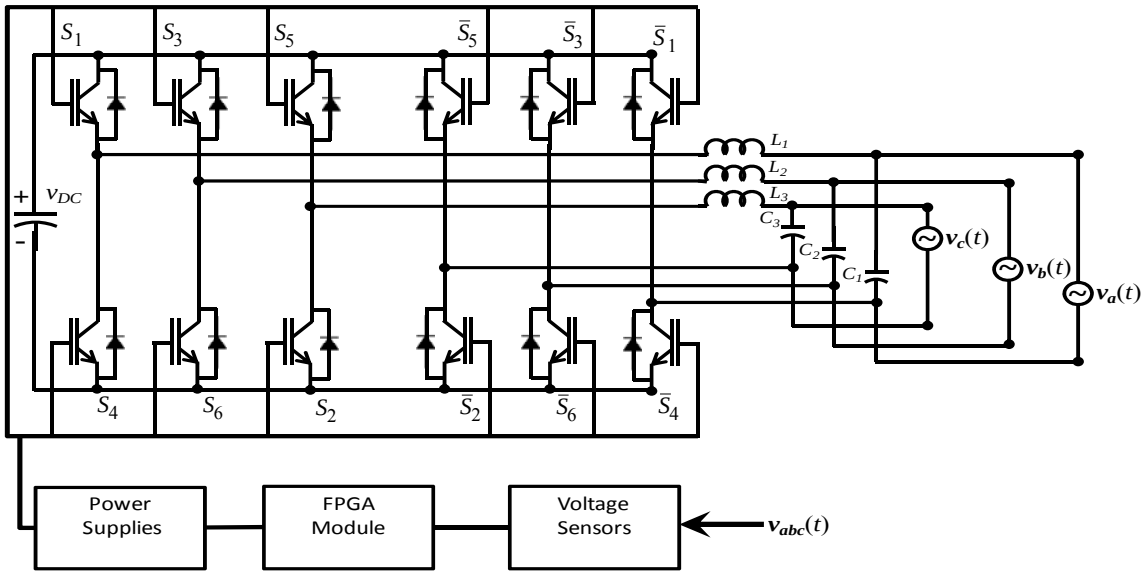

Fig. 4. Three-phase DC/AC voltage source converter.

The single-phase converter is built using four ideal switches (S_1, S_2, S_3 and S_4) and four anti-parallel diodes (D_1, D_2, D_3 and D_4). In the model, sinusoidal at 60 Hz and carrier wave are compared to generate PWM signals. The converter switching frequency was adjusted at 3 kHz. The single-phase inverter is connected to the common 24 VDC source. LC filter block is included to diminish the high frequency harmonics caused by DC to AC conversion; therefore output signal distortion can be reduced. The filter's inductance and capacitance are 31 mH and 1 μF, respectively. The load is rated at 1 kΩ and connected at LC filter output. The simulation model is shown in Fig. 5. The simulation and experimental results are analyzed. Fig. 6a shows that the index harmonic theoretical terms of $v_{ab}(t)$ are $n = 6m \pm 1$, being m any positive integer. That is, $n = 5, 7, 11, 13, \ldots$. To validate (6) Fig. 6b presents the output voltage $v_{ab}(t)$ without LC filter.

V. Experimental Results

A. Single-phase inverter

Fig. 2b shows the result of SPWM that connects to the four switching devices gates firing to generate the sinusoidal voltage at 60 Hz. 4 IGBT's of 160 watts for the implementation are used, Fig. 5.

The line to neutral converter output voltage was stored for a four-channel digital oscilloscope at 500 MHz. Several experiments were conducted with different RLC loads, for exemplifying the steady state converter operation is analyzed. Fig. 7 exhibits that the converter output voltage has a very well quality shape. The output frequency is 59.95 Hz, and a voltage magnitude is 123 volts rms with a RC load.

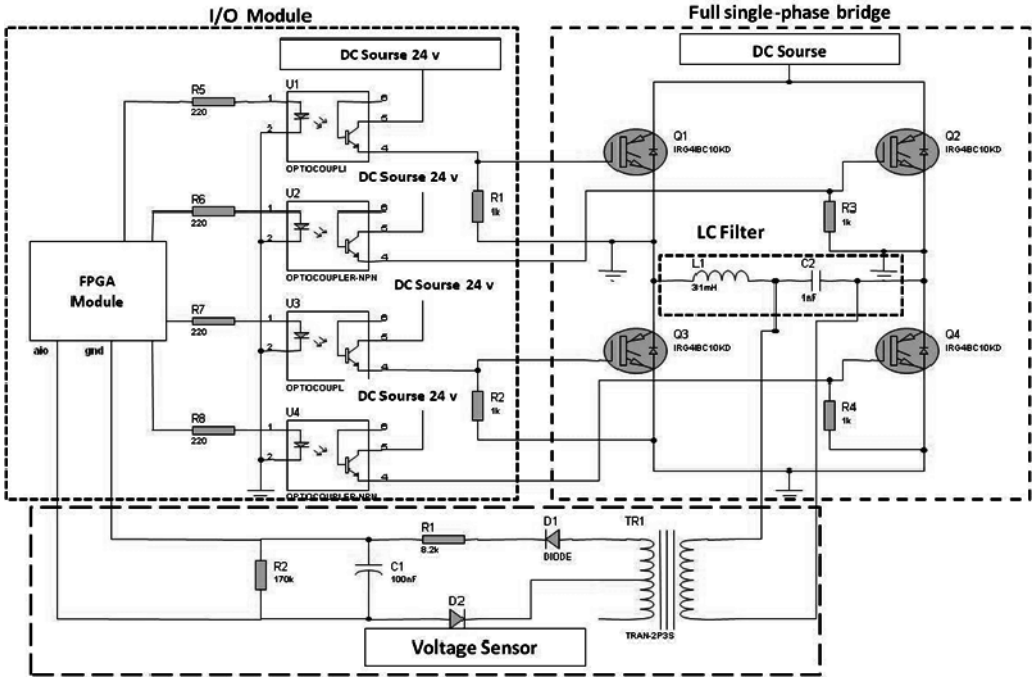

Fig. 5. Single-phase voltage source converter implemented for simulation and laboratory prototype.

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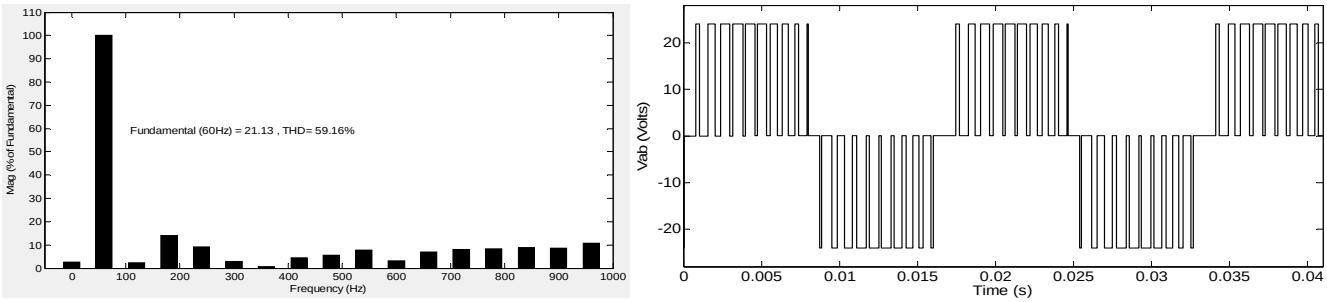

(a) (b)

Fig. 6. Unfiltered output switched voltage (Simulation); (a) harmonic spectra; (b) waveform.

A. Three-phase inverter

Due to the complexity of three-phase inverter, the proposed scheme was implemented in software and hardware devices. Which employs a FPGA-based embedded chip and a processor capable of real-time processing with the following characteristics: DRAM 128 MB, speed frequency 400 MHz, nonvolatile memory 2 GB. One module with 4 analog inputs with a resolution of 16 bits and a sampling frequency 100 KS/s for channel simultaneously and two modules where each one with 8 I/O digital to $1\mu s$. The sampling rate was adjusted to FPGA at $0.0025\mu s$.

The three-phase converter topology is presented in Fig. 4, where FPGA module generates twelve signals (SPWM) similar to Fig. 2b, one for each gate firing of IGBT's. The design of distributed arithmetic used 2541 slides of 14336 possible, 2888 layers of Flip-Flops of 28672 and 22 blocks of RAM.

When the FPGA module receives an external signal, the PWM is adjusting in electrical zero degree to begin the converter operation to phase *a*, which is taken as a reference. The phases *b* and *c* modulated signals are displaced 120º and 240º electrical degrees from *a*. To prevent error accumulation in each cycle digital conducted an update of modulated signals.

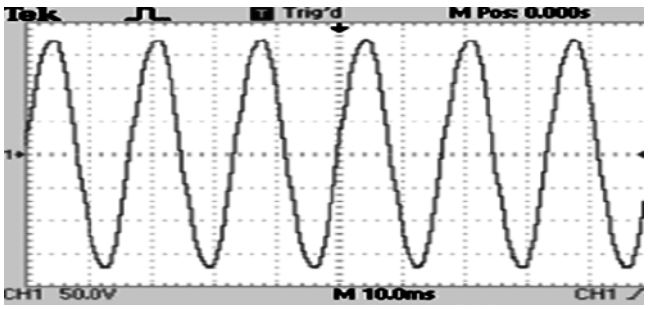

Fig. 7. Single-phase voltage at the coupling transformer for a RC load.

Because the current is dependent on the kind of load, the waveform takes different shape. In this way, to test the power converter operation the device is in face of inductive, capacitive, and resistive loads. Fig. 8 exhibits the inverter current waveform with *RL* load, where the output frequency is closed to 60 Hz in all phases. The current has a sinusoidal shape when the load is *RL*, in this case R = 1.2 KΩ and L = 3.2 mH.

The results show that the voltages are balanced and have high quality waveform, Fig. 9. The switching frequency content is minimized with the inclusion of the LC –filter with the isolating transformer. In Fig's. 9-10 we can see that the output frequency is closed to 60 Hz in the three phases, when load is RL and R respectively.

The experimental results for R and RL loads are presented in the time domain in Fig's. 10-11. Fig's. 10a -and 11a show the steady-state performance, demonstrating that the total harmonic distortion at the output phase voltages is small under balanced load.

Fig's. 10-11 exhibit the harmonic spectrum of the loaded phase voltage v_a. It is possible to see that harmonics are reduced very significantly with respect to the harmonic spectra from unfiltered output switched voltage. Fig's. 10b-11b reveal the excellent steady-state performance with a very low THD and reduced distortions.

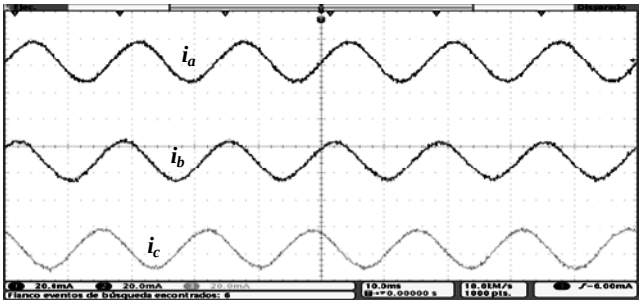

Fig. 8. Three-phase current for a RL load.

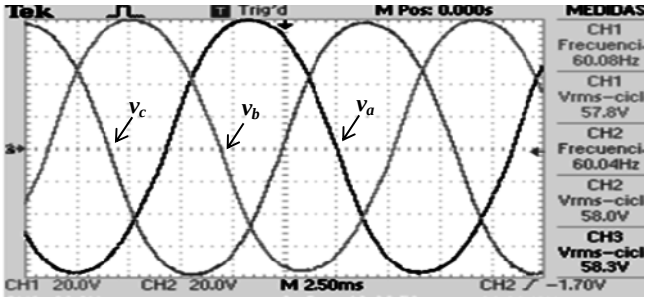

Fig. 9. Three phase voltage at the coupling transformer for a RL load.

Finally, Fig. 12 presents the experimental result of the three-phase output voltage and current from phase *a*, exhibiting reduced distortions for a RL load. These results demonstrate the excellent steady-state performance with a very low THD in accordance with Fig's. 6-12. It has been possible comparing theoretical and laboratory measurements.

VI. Conclusion

Simulations and experimental results of the single and three phase converter are analyzed. These exhibit that the technique works well for all three load types, keeping the output frequency and voltage level within a very acceptable operating margins and with low harmonic content profile, too.

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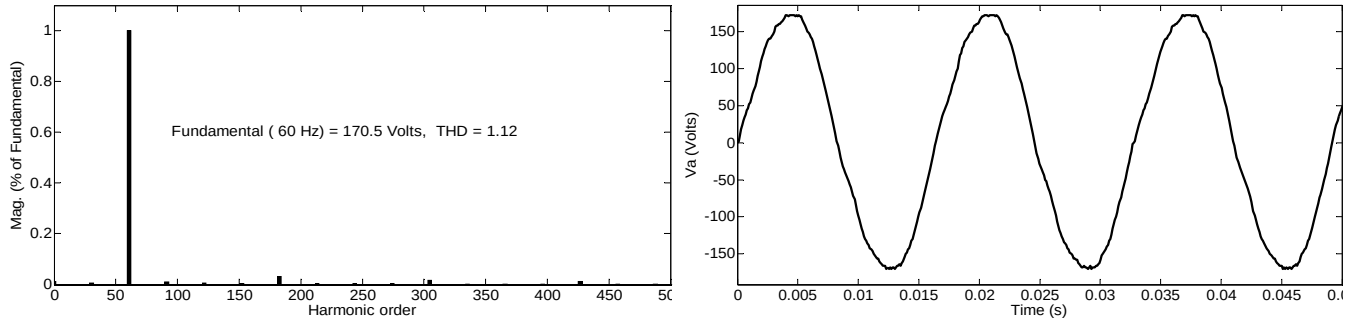
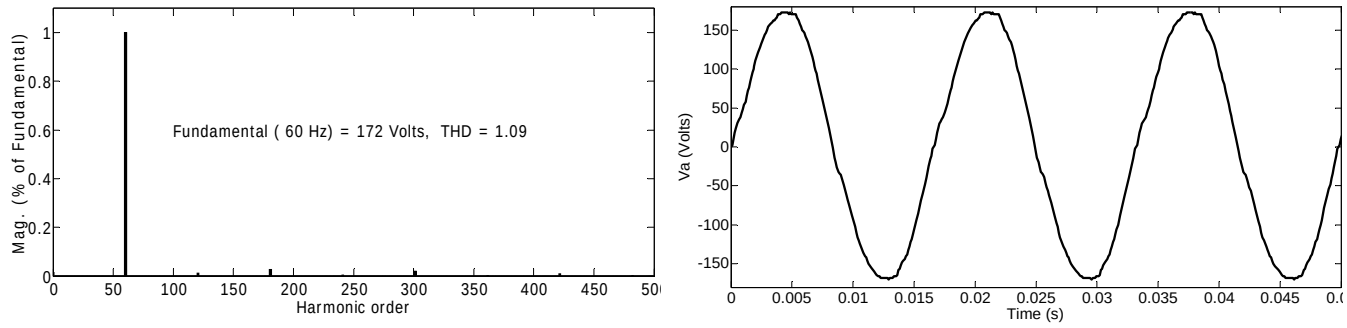


(a) (b)

Fig. 10. Filtered inverter output voltage three-phase for a load R (phase a); (a) voltage harmonic spectrum; (b) waveform.



(a) (b)

Fig. 11. Filtered inverter output voltage three-phase for a load RL (phase a); (a) voltage harmonic spectrum; (b) waveform.

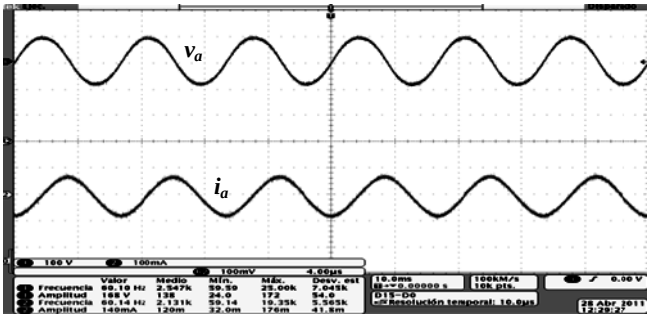


Fig. 12. Voltage and current three phase (phase a) at the coupling transformer for a load RL.

Due to the flexibility of a FPGA, the voltage source converter implementation is feasible and can be fitted with other control algorithms easily, such as adaptive schemes. The complete system for three-phase inverter was designed using a modular system approach, integrated and mounted within a programmable logic device based on FPGA. The scheme was tested by simulations and laboratory prototype, showing very well performance and excellent stability in steady state condition.

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