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Single phase angle tracking method for power switches gating synchronization

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ABSTRACT

This paper proposes a novel method for generating the pulses needed to fire power electronic switches that can be used for single-phase power converters. Simple operations based on the three-phase arctangent method are used within a digital signal controller or microcontroller to generate a sawtooth carrier signal *phi*, with an amplitude of 2pi and concurrent to the period of time of the sinusoidal input. With this signal and using standard Pulse Width Modulation techniques, gating is obtained directly. Two orthogonal signals are the basis of the arctangent method of synchronization; these signals are obtained by numerical differentiation, and normalized using frequency of the same amplitude. This strategy shortens the time consumed. The synchronizing method proposed is validated through MATLAB simulations, and used with several single-phase grid variations, such as sag, swell, flicker, frequency or phase jump. Infinite impulse response (IIR) Butterworth filter is added to take into consideration harmonic contamination on the grid. Experimental results of gating signals are presented to show the proposal's feasibility.

1. Introduction

Distributed generation is gaining acceptance for domestic customers who have more small-scale generation units available, such as photovoltaic cells, wind turbines or fuel cells. In order to connect these power electronic systems to the grid, appropriate gating synchronization of each power switch has to be performed. To achieve this task, zero crossing detectors and time delays have been used for several years as the primary synchronization method in both single- and three-phase systems, but the delay is dependent on frequency. Arctangent gating based method for avoiding this problem is used in [1–4] with good results, but it is specially designed for three-phase systems where it is possible to pass from three measured signals $a(t)$, $b(t)$, and $c(t)$, to two coordinates $\alpha(t)$ and $\beta(t)$, for stationary reference frame. Single phase zero crossing measurement techniques that combine hardware and software methods with low process delay are detailed in [5]; however, the phase error needs pre-filtering and post-processing so that it is reduced to acceptable levels. One method for synchronizing thyristor gating-based power converters that uses adaptive online waveform reconstruction, and fits systems where the frequency of the line might vary is presented in [6], but this method uses a numerical interpolation inside the microcontroller program. Synchronous PLLs have been used in the control of AC systems, and they have become the standard implementation in three-phase applications [7–9]. However, for a single-phase system, there is only one signal to synchronize with, and an orthogonal signal must therefore be created to transform the system from the stationary to the synchronous frame [10]. Efforts to acquire phase and frequency of the signals using control techniques for single-phase systems are exemplified in [11], but the transient time of these schemes is long. Phase angle feedback in mixer phase detectors used to reduce ripple noise and increase synchronization speeds without low-pass filter is presented in [12]; however, an overshoot penalty has to be paid for this increase in synchronizing speed. Applications of digital PLLs in single-phase, grid-connected systems are presented in [13–18]. These schemes use the stationary or rotating coordinate system; nevertheless, they need the generation of a phase shifted signal obtained by lagging the input signal a certain time, which makes the system dependent on the period of the fundamental, or else, they need a PI controller and have to wait the settling time in any variation of the input. The Second Order Generalized Integrator (SOGI) is presented as a good option in the task of obtaining

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an orthogonal system for the application of a PI structure and the generation of the synchronizing signal independently of the grid frequency [19]; nonetheless, it needs to adjust a resonant frequency by the provided frequency of the PLL structure, and it is sensible to voltage offset. An improved version of this PLL is presented in [20]. In this scheme a low pass filter and a subtracter are used to eliminate the offset with good results.

This paper presents a strategy that takes the single-phase power supply voltage, after the typical analog signal conditioning process for limiting it to positive values related to the analog input of the microcontroller or digital signal controller used, and employs plain digital processing operations for obtaining the orthogonal signals $\alpha(t)$ and $\beta(t)$ needed to apply the arctangent method in the detection of the fundamental angle. With this scheme based on a double derivation process from the input signal, the offset added on the signal conditioning is removed, and the deviation that could appear due to successive integrations is eliminated. The arctangent method for synchronization has as its main advantage over the others that it does not require PI controllers for its implementation, and phase is obtained quickly. With these characteristics of getting the quadrature signals within two-sample time per differentiation, and arctangent also within a sample time; the scheme is suitable to be used when variations such as sag, swell, flicker, frequency or phase jump are presented. The ability of this strategy in tracking the angle of the single-phase grid signal through the $\alpha(t)$, and $\beta(t)$ obtained by the derivation process, makes the use of PWM a straightforward solution for gating the electronic switches of the single-phase power systems. This paper presents in Section 2 the arctangent method for a three-phase system and then the way to get the quadrature signals on a single phase grid. Section 3 illustrates the functionality of the proposal by simulation of several possible problems on the system, while Section 4 exemplifies these results with a lab prototype. Finally, Section 5 offers general conclusions on this work.

2. Single phase PLL strategy

A three-phase PLL used in FACTS devices are described in [1–3]. This PLL uses the stationary reference frame for reducing computational costs and helping the system's dynamic performance, obtaining signals $\alpha(t)$ and $\beta(t)$ as illustrated:

$$\begin{bmatrix}\alpha(t)\\ \beta(t)\end{bmatrix} = \begin{bmatrix}\frac{2}{3} & -\frac{1}{3} & -\frac{1}{3}\\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}}\end{bmatrix} \cdot \begin{bmatrix}a(t)\\ b(t)\\ c(t)\end{bmatrix} \tag{1}$$

In this equation, $a(t)$, $b(t)$, and $c(t)$ are the components of a three phase power system, defined by:

$$\begin{bmatrix}a(t)\\ b(t)\\ c(t)\end{bmatrix} = \begin{bmatrix}A\sin(\omega t+\theta)\\ A\sin\left(\omega t+\theta-\frac{2\pi}{3}\right)\\ A\sin\left(\omega t+\theta+\frac{2\pi}{3}\right)\end{bmatrix} \tag{2}$$

When the three-phase system is balanced, the signals $\alpha(t)$ and $a(t)$ have the same phase and frequency, and $\beta(t)$ is in quadrature. The signal $\beta(t)$ leads $\frac{\pi}{2}$ rad the signal $\alpha(t)$. To obtain the instantaneous phase angle ωt of the input signal $a(t)$ using these new coordinates $\alpha(t)$ and $\beta(t)$, the arctangent strategy is employed. This method is based on the relation:

$$\text{angle} = -\tan^{-1}\left(\frac{\alpha(t)}{\beta(t)}\right) \tag{3}$$

Drawing this angle versus time, a sawtooth signal of two times the frequency of fundamental one $a(t)$ is obtained. This angle signal

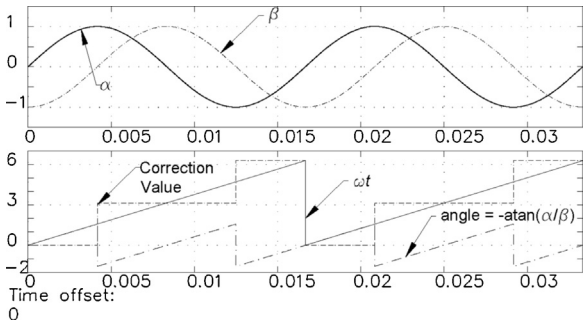

Fig. 1. PLL strategy.

Table 1
Correction value for PLL.

Sign of $\alpha(t)$	Sign of $\beta(t)$	Correction value
−	−	2π
−	+	π
+	−	0
+	+	π

is centered to the origin, and leads $\frac{\pi}{2}$ rad to $\alpha(t)$ as presented in Fig. 1. In order to have the sawtooth carrier signal compared with the angle for gating a power switch, a correction value determined by the signs of $\alpha(t)$ and $\beta(t)$ is added to (2), as defined in Table 1. The resulting signal is presented as ωt.

This paper presents a similar strategy, specific to single-phase systems. In this case there is only one signal available to be taken for the microcontroller, and it is established as the input signal $u(t)$, corresponding to a function of the form:

$$u(t) = \frac{A}{2}\sin(\omega t) + \frac{A}{2} \tag{4}$$

As a microcontroller or digital signal controller (DSC) is used, $u(t)$ is a positive signal related to the analog input of the controller. Thus, its maximum value corresponds to the maximum input allowed by the analog to digital input, and is labeled A. The offset is chosen to be $\frac{A}{2}$ in order to have the input signal at the maximum allowable variation. If we want to use the arctangent method, two orthogonal signals $\alpha(t)$ and $\beta(t)$ obtained from the input signal $u(t)$ are needed. $\alpha(t)$ and $\beta(t)$ should be AC for arctangent method implementation. By using a derivative operator, it can be observed that $\frac{d}{dt}u(t)$ is an AC signal without offset,

$$\frac{d}{dt}u(t) = \frac{\omega}{2}A\cos(\omega t) \tag{5}$$

Normalizing function (5) with $\frac{\omega}{2}$, the signal $\beta(t)$ appears with same amplitude as the input but without offset, as

$$\beta(t) = \left(\frac{2}{\omega}\right)\frac{d}{dt}u(t) = A\cos(\omega t) \tag{6}$$

Using the derivative operator with this version of $\beta(t)$, another AC signal without offset is obtained as presented

$$\frac{d}{dt}\beta(t) = -\omega A\sin(\omega t) \tag{7}$$

Leading this signal π rad (change in the sign), and normalizing using ω, we obtain the signal $\alpha(t)$, as illustrated in (8). This version of $\alpha(t)$ has the same amplitude as the input

$$\alpha(t) = \left(\frac{-1}{\omega}\right)\frac{d}{dt}\beta(t) = A\sin(\omega t) \tag{8}$$

These two orthogonals can be used for the arctangent method, as they are signals without offset as illustrated in Fig. 1. In order to implement these differentiations inside the microcontroller or digital signal controller, the input signal is sampled with period T, so

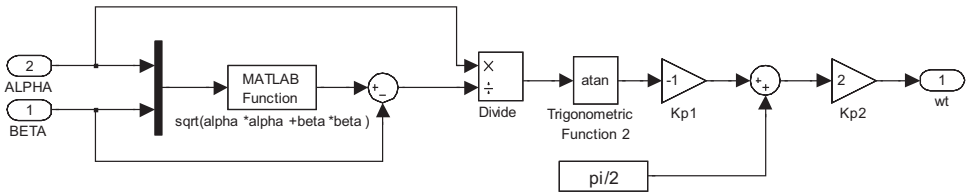

Fig. 2. Single-phase PLL proposed strategy simulink model.

Table 2
IIR Butterworth filter parameters.

k1	−0.00036457	a21	−1.981622
k2	0.00035909	a31	0.9830802
k3	0.0003554	a22	−1.951867
k4	0.0188176	a32	0.9533035
b21	2	a23	−1.931794
b22	2	a33	0.9332156
b23	2	a24	−0.962365

it is considered $u(nT)$. Thus, it is needed to develop digital operations. Differentiation operation can be approximated in discrete time using backward Rectangular Rule, which is presented in (9) in z transform for $\beta(z)$, and the corresponding Linear Constant Coefficient Difference Equation defined by (10) for $\beta(nT)$, and similarly in (11) for $\alpha(z)$, and (12) for $\alpha(nT)$, considering the change in the sign. Eqs. (10) and (12) are the ones implemented on the microcontroller for obtaining $\beta(nT)$ and $\alpha(nT)$

$$\beta(z) = \left[\frac{z-1}{zT}\right] u(z) \left(\frac{2}{\omega}\right) \tag{9}$$

$$\beta(nT) = \left(\frac{1}{T}\right) (u(nT) - u(nT-1)) \left(\frac{2}{\omega}\right) \tag{10}$$

$$\alpha(z) = -\left[\frac{z-1}{zT}\right] \beta(z) \left(\frac{1}{\omega}\right) \tag{11}$$

$$\alpha(nT) = -\left(\frac{1}{T}\right) (\beta(nT) - \beta(nT-1)) \left(\frac{1}{\omega}\right) \tag{12}$$

By using these digital versions of $\alpha(nT)$ and $\beta(nT)$ the arctangent method can be implemented in a straightforward manner, synchronizing the PLL's zero output with respect to the startup of the $\alpha(nT)$ signal, when the $\beta(nT)$ signal presents its minimum value, as illustrated in Fig. 1. The scheme can be reduced to Eq. (13) to avoid verifying the polarities of α and β, and making it robust to variations in the input signal. This is the strategy followed in this paper, as depicted in Fig. 2

$$\omega t = 2\left[-\tan^{-1}\left(\frac{\alpha}{\sqrt{\alpha^2+\beta^2}-\beta}\right) + \frac{\pi}{2}\right] \tag{13}$$

3. Case study

In order to verify the effectiveness of the proposal, several tests have been carried out. A seventh order infinite impulse response (IIR) Butterworth filter, designed for a 15 kHz sampling rate, 180 Hz as the stop frequency and 70 Hz as the pass frequency is added to avoid harmonic contamination, and the structure performed in Direct Form II, with second order sections is presented in Fig. 3, and the corresponding values included in Table 2.

3.1. Sag and swell

A simulation with a grid signal with the parameters of Table 3 is illustrated in Fig. 4(top). This signal presents a steady-state grid

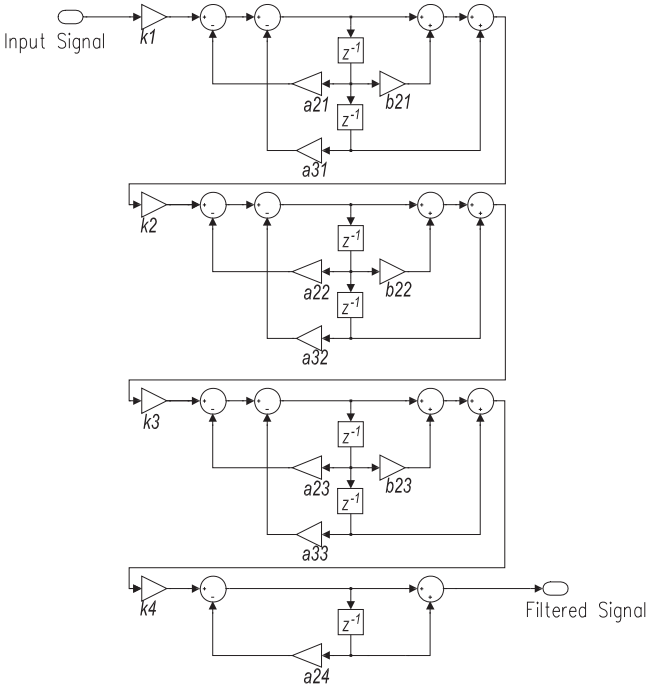

Fig. 3. IIR Butterworth filter.

Table 3
Grid signal parameters.

Frequency (Hz)	60
Amplitude of fundamental (V)	$127\sqrt{2}$
Nominal voltage	Cycles 1 and 2
Sag 20%	Cycles 3 and 4
Swell 20%	Cycles 5 and 6
Nominal voltage	Cycles 7 and 8

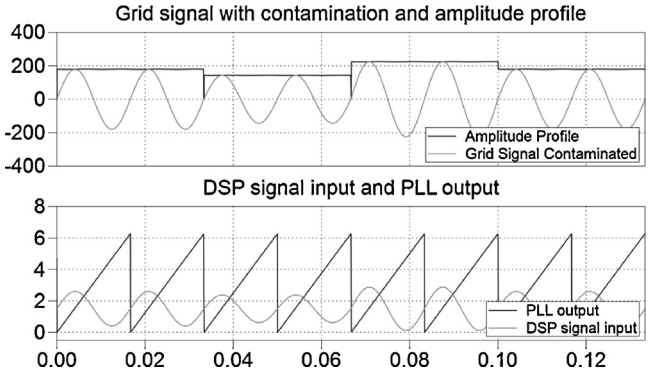

Fig. 4. (Top) Grid signal contaminated, and amplitude profile of grid signal. (Bottom) PLL signal obtained with the strategy of this paper and DSP signal input.

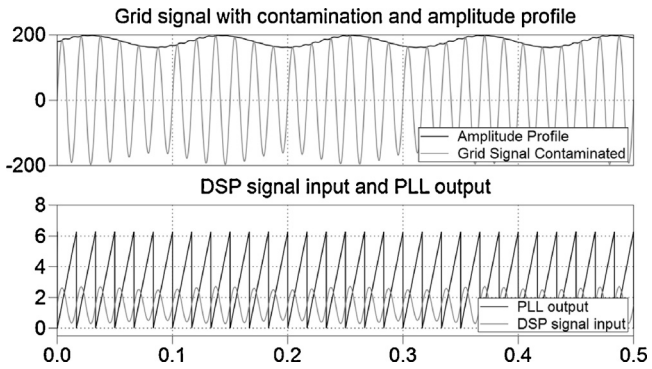

Fig. 5. (Top) Grid signal with flicker, and amplitude profile of grid signal. (Bottom) PLL signal obtained with the strategy of this paper and microcontroller signal input.

voltage affected by a two-cycle sag of 20% of amplitude, then by a two-cycle swell of 20% of amplitude, and return to steady state. It is noticeable that the PLL signal obtained with the contaminated signal is still obtaining the frequency and phase angle regardless of these disturbances, as presented in Fig. 4 (bottom).

3.2. Flicker noise

This test was performed by using a grid signal contaminated with an 8.8 Hz sinusoidal signal. This contamination is considered the most sensitive frequency for the human eye and nervous system [21]. The critical magnitude is of about 0.3% of the fundamental [22]. In order to verify the capability of the proposed strategy for getting phase and frequency synchronization, the magnitude of the flicker has been expanded to 10% of the fundamental. A grid signal with flicker noise along with the voltage's amplitude profile is presented in Fig. 5(top). The lower part of this figure illustrates the microcontroller input and the PLL output. As in the previous case, the PLL signal still obtains the frequency and phase angle of the input signal.

3.3. Frequency jump

A frequency jump takes place mainly at the borders of systems with different frequency signal. A jump from 60 Hz to 50 Hz starting at a 2.8 cycles is exemplified through Fig. 6. The transition is seen as a discontinuity with 2 sampling time durations due to second derivative calculation, and a slight reduction in the PLL slope is noticed.

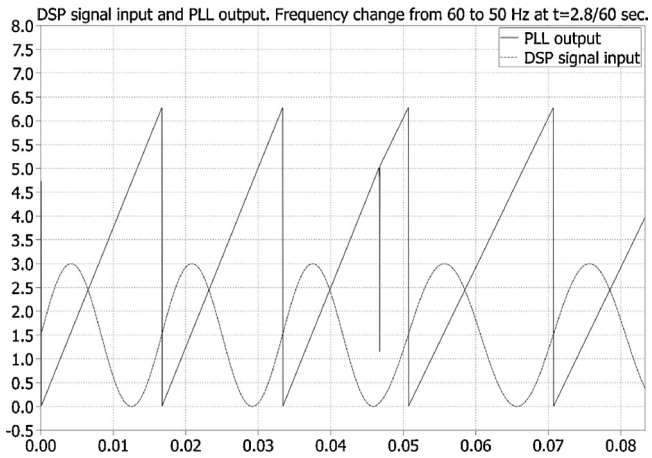

Fig. 6. Step change in frequency and PLL output.

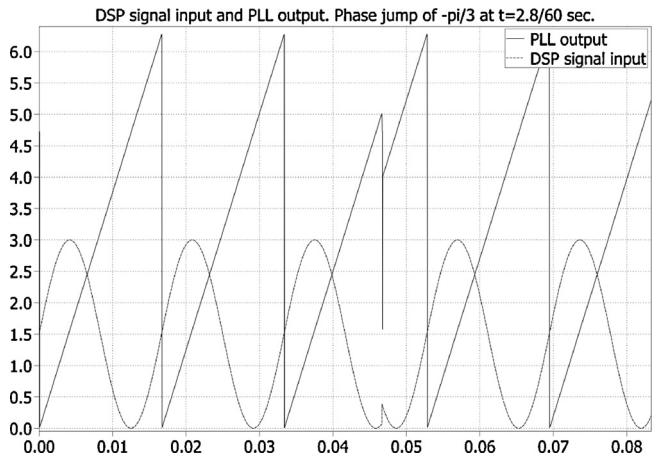

Fig. 7. Phase jump of $\frac{\pi}{3}$ lagging the DSP signal input and PLL output.

3.4. Phase jump

A phase jump may occur if a large load is suddenly connected, or if there is a fault in the grid system. Lag and lead of $\frac{\pi}{3}$ rad are illustrated in Figs. 7 and 8, respectively. The jump occurs at a 2.8 cycle in both cases. The transition in phase is perceived as a discontinuity with 2 sampling time durations due to second derivative calculation, but again, there is no change in the PLL slope. The end of the DSP signal input concurs at the end of the PLL output in both phase jumps as expected.

3.5. Harmonic contamination

One of the main useful techniques when using a microcontroller or digital signal processor in an application is the ability of implementing filtering as part of the code. With the addition of the IIR Butterworth filter of Fig. 3, the proposed strategy of this paper has been under harmonics of a single frequency as presented in Fig. 9(a) for the fifth harmonic with fundamental amplitude /5, Fig. 9(b) for seventh harmonic with fundamental amplitude /7, Fig. 9(c) for 11th harmonic with fundamental amplitude /11, and Fig. 9(d) 13th harmonic with fundamental amplitude /13. In all cases we see the sawtooth signal without effect produced by the harmonics.

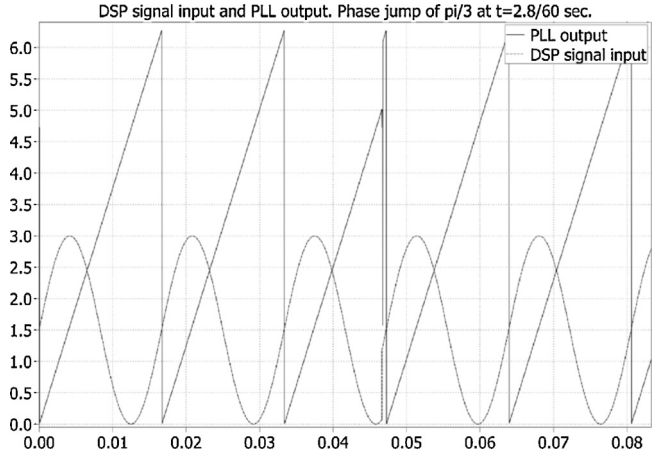

Fig. 8. Phase jump of $\frac{\pi}{3}$ leading the DSP signal input and PLL output.

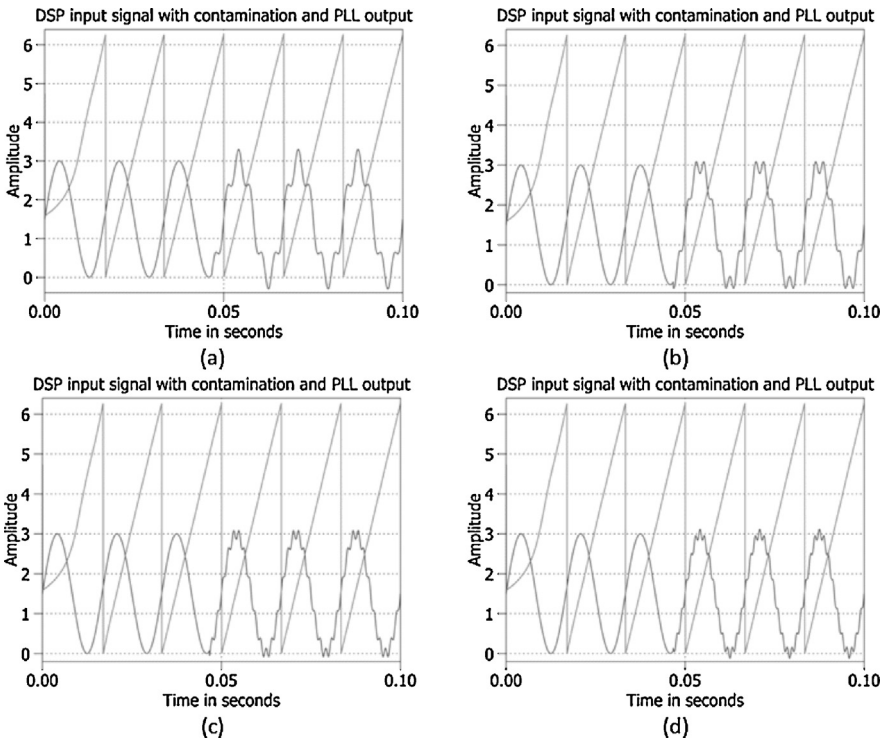

Fig. 9. PLL output and DSP signal with contamination as: (a) fifth harmonic with fundamental amplitude /5, (b) seventh harmonic with fundamental amplitude /7, (c) 11th harmonic with fundamental amplitude /11, and (d) 13th harmonic with fundamental amplitude /13.

4. Prototype results

The method proposed in this paper was implemented in a lab prototype with a LM3S8962, which is a 32 bits ARM Cortex-M3 microcontroller from Texas Instruments. The microcontroller's main clock was set to 50 MHz and the sampling frequency to 15 kHz. The algorithm was implemented in fixed-point arithmetic using IQMath [23], to enhance execution time in the system. As the purpose of this paper is to show the implementation of the PLL strategy, the prototype is simple and depicted in Fig. 10. The results presented on the following images were captured in a Tektronix TDS2002 oscilloscope. The operations (10) and (12) are the ones that need to save memory data for their implementation, and have an execution time of 7.5 μs on the microcontroller running at a frequency of 50 MHz. Fig. 11(a) illustrates the result of executing the algorithm at Reference B of the oscilloscope. The result is similar to the one of Fig. 1. This signal is passed through a digital to analog converter (DAC) to verify the strategy of the paper. The flat spot at the bottom of this reference is related to the low significant bits of the DAC used on the implementation. The other parts of Fig. 11 illustrate examples of gating signals at a specific activation angle. They can be used for activating power switches used for the construction of power electronic devices synchronized to the electrical grid. Fig. 11(b) presents a firing signal at $\frac{\pi}{2}$ rad from reference signal. Standard PWM comparison of this angle with the sawtooth signal obtained with the proposed method is used for generating the gating signal. In this study the width of the gating signal was not taken into consideration because the main objective was to synchronize the firing circuits to zero on the input signal. Fig. 11(c), and Fig. 11(d) depict the gating signal for an activation angle of $\frac{5\pi}{6}$ rad and $\frac{3\pi}{2}$ rad, respectively. It is important to note that activation angle can vary from 0 to 2π, which is one of the main advantages of the proposed strategy.

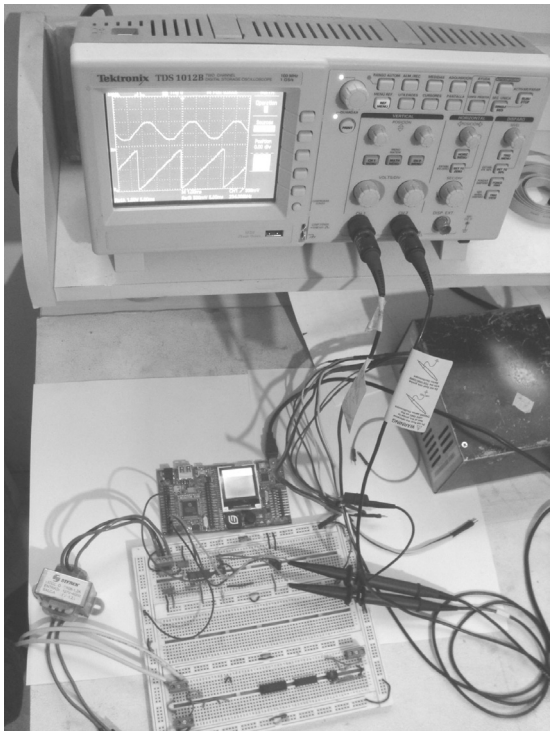

Fig. 10. Lab's signal verification.

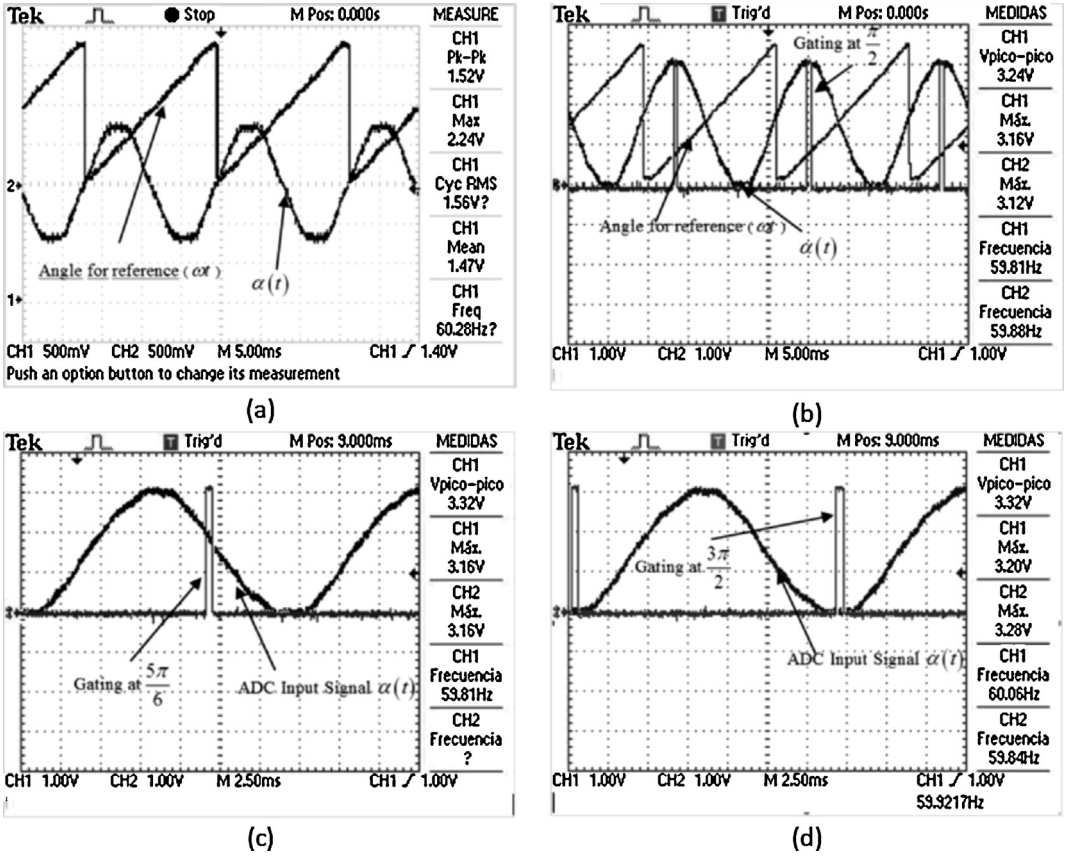

Fig. 11. Implementation signals: (a) signals $\alpha(t)$ and PLL output of the proposed method, (b) gating signal present at $\frac{\pi}{2}$ rad from reference signal, (c) gating signal present at $\frac{5\pi}{6}$ rad from reference signal, and (d) gating signal present at $\frac{3\pi}{2}$ rad from reference signal.

5. Conclusions

This paper has presented a very efficient way to synchronize electronic switches for their use on power converters to the single-phase grid. In general, the signals obtained from typical sensors should be pre-filtered, conditioned and amplified to eliminate undesirable noise levels. This is performed via integrated electronics to sensors or by means of external electronics, from which are obtained the signals to be digitally processed on the microcontroller or digital signal controller. Noise is always a problem in practical applications. Thus, a Butterworth low-pass filter is recommended. By using the strategy described in this paper, the effort to obtain the angle of the input signal is reduced, and the time for this task is shortened. This can be done in any microcontroller with capabilities of computing an arctangent function. One of the main advantages of this method is that the firing angle can be spread from 0 to 2π, which allows this scheme to be used on any AC–DC or DC–AC converter. Typical variations on the input, such as sag, swell, flicker noise, phase of frequency jump, have been used to test the PLL routine with appropriate results. Harmonic contamination is always a point to consider when we think on power converters, but a simple Butterworth low-pass filter would help to have good results. Prototype results of gating signals are presented to probe the suitableness of the method. This strategy can be easily used by people encouraged to design single-phase tied power converters, and students who traditionally spend a long time trying to synchronize their power semiconductor devices to the zero crossing of the alternating current.

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